# TWO-STEP SOURCE SIDE IMPLANT FOR IMPROVING SOURCE RESISTANCE AND SHORT CHANNEL EFFECT IN DEEP SUB-0.18μm FLASH MEMORY TECHNOLOGY

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**ABSTRACT**

Methods of forming flash memory EEPROM devices having lightly doped source region near the critical gate region and a heavily doped source region away from the critical gate region. In a first embodiment a first source mask is formed exposing source regions and portions of the gates and implanting n dopant ions, replacing the first source mask with a second source mask that exposes a portion of the source regions and implanting $n^-$ dopant ions. In a second embodiment a source mask is formed exposing a portion of the source regions and implanting $n^-$ dopant ions.